AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

What is claimed is:

Claim 1 (currently amended): A method for forming a floating gate, comprising:

providing a semiconductor substrate, wherein a gate dielectric layer and a conducting layer are sequentially formed on the semiconductor substrate;

forming a patterned hard mask layer having an opening on the semiconductor substrate, wherein a portion of the surface of the conducting layer is exposed through the opening;

forming a spacer on a sidewall of the opening;

removing the patterned hard mask layer;

forming a conducting spacer on a sidewall of the spacer;

and sequentially removing the ~~exposing~~ exposed conducting layer and the ~~exposing~~ exposed gate dielectric layer.

Claim 2 (original): The method for forming a floating gate of claim 1, wherein the hard mask layer is a silicon nitride layer.

Claim 3 (original): The method for forming a floating gate of claim 1, wherein the gate dielectric layer is gate oxide layer.

Claim 4 (original): The method for forming a floating gate of claim 1, wherein the conducting layer is a poly-layer.

Claim 5 (original): The method for forming a floating gate of claim 1, wherein the spacer is an insulating layer.

Claim 6 (original): The method for forming a floating gate of claim 5, wherein the insulating layer is silicon oxide layer.

Claim 7 (original): The method for forming a floating gate of claim 1, wherein the material of the insulating layer is different from the hard mask layer.

Claim 8 (original): The method for forming a floating gate of claim 1, wherein the conducting spacer is a poly-layer.

Claim 9 (currently amended): A method for forming a floating gate, comprising:

providing a semiconductor substrate; sequentially forming a gate dielectric layer and a first conducting layer on the semiconductor substrate;

sequentially forming a hard mask layer and a patterned resist layer having a first opening on the first conducting layer, wherein a portion of the hard mask layer is exposed through the opening;

etching the hard mask layer to form a second opening using the patterned resist layer as a mask;

removing the patterned resist layer;

conformally forming an insulating layer on the surface of the hard mask layer, wherein the second opening is filled with the insulating layer;

anisotropically etching the insulating layer to form a first spacer on a sidewall of the second opening; removing the hard mask layer;

conformally forming a second conducting layer on the surface of the first conducting layer and the first spacer;

anisotropically etching the second conducting layer to form a second spacer on a sidewall of the first spacer;

sequentially removing the ~~exposing~~ exposed first conducting layer and the ~~exposing~~ exposed gate dielectric layer, wherein a floating gate consists of a first conducting layer and the second spacer.

Claim 10 (original): The method for forming a floating gate of claim 9, wherein the gate dielectric layer is a gate oxide layer.

Claim 11 (original): The method for forming a floating gate of claim 9, wherein the first conducting layer is a poly-layer.

Claim 12 (original): The method for forming a floating gate of claim 9, wherein the hard mask layer is a silicon nitride layer.

Claim 13 (original): The method for forming a floating gate of claim 9, wherein the insulating layer is a silicon oxide layer.

Claim 14 (original): The method for forming a floating gate of claim 9, wherein the material of the insulating layer is different from the hard mask layer.

Claim 15 (original): The method for forming a floating gate of claim 9, wherein the second conducting layer is a poly-layer.

Claim 16 (original): The method for forming a floating gate of claim 9, wherein a method of the anisotropically etching is a plasma dry-etching process.

Claims 17-22 (canceled)

Claim 23 (new): The method for forming a floating gate of clam 1, wherein the floating gate consists of the conducting layer and the conducting spacer.